☐ **1.** Device design and process integration for SiGeC and Si/SOI bipolar transistors
Haralson, Erik, Jan 2004
...epitaxial SiGeC base, in situ doped **polysilicon emitter**, nickel silicide,LOCOS isolation...simultaneousformation of NiSi on the in situ doped **polysilicon emitter**. High-resolution x-ray diffraction...epitaxial SiGeC base, in situ doped **polysilicon emitter**, nickel silicide, LOCOS isolation...
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...lt;100>, <111>, and <110> channeling directions with the same set of parameters for boron, phosphorus, and **arsenic** implants [15]. This model also is accurate for other implant species such as BF2, F, Al, Ge, In, Sb, etc. [16]. For most MC...
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7. High Frequency Characterization and Modeling of SiGe Heterojunction Bipolar Transistors
Malm, B. Gunnar, Jan 2002
...low-frequency noise in **polysilicon emitter** bipolar transistors...5–10 keV) **antimony** (Sb) implantation...Passivation of **Polysilicon Emitter** Bipolar Transistors...Phosphorous Doped **Polysilicon Emitter**: Optimization...implantation of **antimony** (Sb) was combined...
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8. TUNEABLE SEMICONDUCTOR DEVICE
FREEMAN, Gregory, G. / RIEH, Jae-Sung / SHERIDAN, David, C. / ST.ONGE, Stephen, A. / STRICKER, Andreas, D. / VOLDMAN, Steven, H. / INTERNATIONAL BUSINESS MACHINES CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Dec 2005
...sub-collector 112such as Phosphorus, **Arsenic**, or **Antimony**. The doped level 112,113 controls...limited to P or As but can be **Antimony** or other e-type implants...shown in Figure 5, below the **polysilicon emitter** 130 is a p++ source/drain...
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☐ **12.** COMPLEMENTARY ANALOG BIPOLAR TRANSISTORS WITH TRENCH-CONSTRAINED ISOLATION DIFFUSION
WILLIAMS, Richard, K. / CORNELL, Michael, E. / CHAN, Wai, Tien / ADVANCED ANALOGIC TECHNOLOGIES, INC., *PATENT COOPERATION TREATY APPLICATION*, Feb 2004
...N-type dopant such as **antimony** or **arsenic** is implanted through...high concentration of **arsenic** is used to form the...may also occur using **antimony** as the dopant species...slow-diffusing dopant such as **antimony** or **arsenic**, and P buried layer...
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☐ **14.** IMPLEMENTATION OF A SILICON CONTROL CHIP FOR Si/SiC HYBRID OPTICALLY ACTIVATED HIGH POWER SWITCHING DEVICE
BHADRI, PRASHANT R., Jan 2002
In avionic systems, data integrity and high data rates are necessary for stable flight control. Unfortunately, conventional electronic control systems are susceptible to electromagnetic interference (EMI) that can reduce the clarity of flight control ...
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☐ **15.** Bipolar transistor free from leakage current across thin base region and process of fabrication thereof
Sato, Fumihiko / NEC CORPORATION, *EUROPEAN PATENT*, Mar 1996
...substrate 1 is regulated to be about 15 ohm-cm. A heavily **arsenic**-doped buried layer 2 is formed in a surface portion...temperature, and is oriented to (100) crystal direction. **Arsenic** or **antimony** is diffused into a part of the lightly doped p-type...
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☐ **16.** JP Publications - Grouped (4/5/05) 1 [PDF-90K]
Apr 2005
...Sinclair and J. D. Plummer, "Morphological Studies of **Polysilicon Emitter** Contacts," Proceedings Materials Research Society, 37...and J. D. Plummer, "Physics, Technology and Modeling of **Polysilicon Emitter** Contacts for VLSI Bipolar Transistors," IEEE Transactions...
[http://snf.stanford.edu/staff/plummer/JDP-PUBS.PDF]
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☐ **17.** Manufacturing method of a bipolar transistor
Sawada, Shigeki / Matsushita Electronics Corporation, *EUROPEAN PATENT*, Oct 1990
...layer 20 from the N+ **polysilicon emitter** electrode 31 through...100 Torr. Using **antimony** of which diffusion...smaller than that of **arsenic**, by performing epitaxial...to

limit to the **antimony**, but by using **arsenic**, for example, it...
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☐ **18.** High Frequency Characterization and Modeling of SiGe Heterojunction Bipolar Transistors
Malm, B. Gunnar, Apr 2002
...low-frequency noise in **polysilicon emitter** bipolar transistors...5–10 keV) **antimony** (Sb) implantation...Passivation of **Polysilicon Emitter** Bipolar Transistors...Phosphorous Doped **Polysilicon Emitter**: Optimization...implantation of **antimony** (Sb) was combined...
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☐ **20.** A complementary bipolar technology family with a vertically integrated PNP for high-frequency analog - Electron Devices, IEEE ... [PDF-54K]
Apr 2004
...vertical isolation. Next, the n-type **antimony** buried layer for the NPN is implanted...is then implanted with boron and **arsenic** for the emitter regions. Furnace...implantation and annealing of n (**antimony**) and p (boron) buried layer, and...
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☐ **21.** COMPLEMENTARY BIPOLAR POLYSILICON EMITTER DEVICES
ROBINSON, Derek, W. / KRIEGER, William, A. / MARTINEZ, Andre, M. / McDEVITT, Marion, R. / ANALOG DEVICES, INC., *PATENT COOPERATION TREATY APPLICATION*, Aug 1993
i - 1˜ COMPLEMENTARY BIPOLAR **POLYSILICON EMITTER** DEVICES Field of the Invention The present invention...e., buried collector) 44, is formed by N-type (e.g., **arsenic**, **antimony**, or phosphorous) ion implantation (doping). Then, an...
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☐ **22.** STRUCTURE AND FABRICATION OF BIPOLAR TRANSISTORS
BULUCEA, Constantin / GRUBISICH, Michael, J. / NATIONAL SEMICONDUCTOR CORPORATION, *EUROPEAN PATENT*, Aug 1996
...layer 12. In the device of Fig. 1, n+ emitter 18, which is formed by dopant outdiffusion from n+ polycrystalline silicon ("**polysilicon**") **emitter** contact 20 so as to be self-aligned to emitter contact 20, overlies p intrinsic base 22. The transistor has two extrinsic...
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☐ **23.** USE OF OBLIQUE IMPLANTATION IN FORMING EMITTER OF BIPOLAR TRANSISTOR
CHEN, Hung-Sheng / TENG, Chih, Sieh / NATIONAL SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 1997
...collector contact zone 24, and **polysilicon emitter** contact 36. N- emitter extension...of opening 40. See Fig. 3c. **Arsenic** is then introduced through...26, must be done before the **arsenic** doping employed in creating...diffuses considerably faster than **arsenic**. Any high-temperature operation...
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☐ **24.** A PROCESS FOR MANUFACTURING IC-COMPONENTS TO BE USED AT RADIO FREQUENCIES
NORSTRÖ / M, Hans / NYGREN, Stefan / TYLSTEDT, Ola /

TELEFONAKTIEBOLAGET LM ERICSSON, *PATENT COOPERATION TREATY APPLICATION*, Jan 1999
...constituted of for example an ion implanted layer of **arsenic** or **antimony**, is lithographically defined, after which an epitaxial...surface of the plate. This layer is implanted with **arsenic** in order to become type N+ and will after annealing...
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☐ **25.** BIPOLAR TRANSISTOR HAVING A COLLECTOR REGION WITH SELECTIVE DOPING PROFILE AND PROCESS FOR MANUFACTURING THE SAME
GRUBISICH, Mike / BULUCEA, Constantin / NATIONAL SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Jul 1997
...buried n+ collector layer 44 along the substrate/epi interface, and field-isolation region 46 of the trench type. N+ **polysilicon emitter** contact 48 contacts n+ emitter 50 in a self-aligned manner. The transistor further includes p base layer 52, a pair of...
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☐ **26.** STRUCTURE AND FABRICATION OF BIPOLAR TRANSISTORS
BULUCEA, Constantin / GRUBISICH, Michael, J. / NATIONAL SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Mar 1996
...layer 12. In the device of Fig. 1, n+ emitter 18, which is formed by dopant outdiffusion from n+ polycrystalline silicon ("**polysilicon**") **emitter** contact 20 so as to be self-aligned to emitter contact 20, overlies p intrinsic base 22. The transistor has two extrinsic...
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☐ **27.** Bipolar transistor and photoelectric conversion apparatus using the same
Morishita, Masakazu / CANON KABUSHIKI KAISHA, *EUROPEAN PATENT*, Oct 1990
...formed between a **polysilicon emitter** region and a monocrystalline...formed between a **polysilicon emitter** region and a monocrystalline...phosphorus (Ph), **antimony** (Sb) or **arsenic** or p type obtained...present between a **polysilicon emitter** region and a monocrystalline...
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☐ **28.** Fabricating a semiconductor structure
Akcasu, Osman Ersed / FAIRCHILD SEMICONDUCTOR CORPORATION, *EUROPEAN PATENT*, Dec 1988
...preferred embodiment, region 12 is doped with **arsenic** to a concentration of approximately 1...sup6] atoms per cubic centimeter of **arsenic** or phosphorus. Next, and not shown in...should be also thick enough to mask the **arsenic** implant for self-aligned p-n junction...
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☐ **29.** Ion implantation to increase emitter energy gap in bipolar transistors
Anand, Kranti / Strain, Robert J. / FAIRCHILD SEMICONDUCTOR CORPORATION, *EUROPEAN PATENT*, Jan 1986
...the base to the adjacent **polysilicon emitter** of a bipolar transistor...includes the step of doping the **polysilicon emitter** region with oxygen thereby...donor impurity, such as **arsenic** or **antimony**, are implanted into a region...
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☐ **30.** Method for manufacturing a BI-CMOS device
Ogura, Seiki / Rovedo, Nivo / International Business Machines Corporation, *EUROPEAN PATENT*, Jun 1990
...without masking, and **arsenic** implant in predetermined...Self-Aligned Narrow Width **Polysilicon-Emitter** Transistors of an...phosphorous as well as **arsenic** in the N+ source/drain...an **arsenic** (As) or **antimony** (Sb) implant in the...both cases. Now the **polysilicon emitter** and FET gate electrodes...
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☐ **31.** Method for fabricating a bipolar transistor
Pollock, Larry Joseph / Brown, George William / SYNERGY SEMICONDUCTOR CORPORATION, *EUROPEAN PATENT*, Oct 1989
...material is formed using **arsenic** or **antimony** as the dopant. This buried...simultaneously form the **polysilicon emitter** and collector contacts 52...preferred embodiment, the **polysilicon emitter** 52 is deposited over the...
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☐ **32.** METHOD OF MANUFACTURING HIGH PERFORMANCE BIPOLAR TRANSISTORS IN A BICMOS PROCESS
DARMAWAN, Johan, A. / NATIONAL SEMICONDUCTOR CORPORATION, *EUROPEAN PATENT*, Jul 1996
...the tapering of the foot of the **polysilicon emitter**, is controlled when the polysilicon...for a bipolar transistor having a **polysilicon emitter** adjacent to silicon substrate. Etching...Bipolar transistor 360 includes a **polysilicon emitter** 310 adjacently overlying substrate...
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☐ **33.** Narrow band gap base heterojunction bipolar transistors using SiGe alloys
Iyer, S.S. / Patton, G.L. / Harame, D.L. / Stork, J.M.C. / Crabbe, E.F. / Meyerson, B.S., *Thin Solid Films*, Jan 1990
...deposited epitaxially without breaking vacuum. **Antimony** and gallium were used during the deposition as...of Si/SiGe junctions was produced by diffusing **arsenic** from a **polysilicon emitter** into an epitaxially deposited base. Silicon and...
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☐ **34.** Semiconductor bipolar device and method of manufacturing the same
Ishigaki, Yoshiyuki / Honda, Hiroki / Uga,Kimiharu / Ishida, Masahiro / MITSUBISHI DENKI KABUSHIKI KAISHA, *EUROPEAN PATENT*, Apr 1995
...polycrystalline silicon doped with **arsenic** (As). Emitter electrode 515...polycrystalline silicon doped with **arsenic**. The surface of interconnection...as a mask, impurity such as **antimony** (Sb) is implanted into p...563. Referring to Fig. 79, **arsenic** is implanted into the whole...
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☐ **35.** METHOD OF MANUFACTURING HIGH PERFORMANCE BIPOLAR TRANSISTORS IN A BICMOS PROCESS
DARMAWAN, Johan, A. / NATIONAL SEMICONDUCTOR CORPORATION, *PATENT COOPERATION TREATY APPLICATION*, Feb 1996

...tapering of the foot of the **polysilicon emitter**, is controlled when the...bipolar transistor having a **polysilicon emitter** adjacent to silicon substrate...equal to the thickness of **polysilicon emitter** 310 and thin polysilicon...exemplary BiCMOS process, n' **antimony** implant layers may be buried...
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☐ **36.** Bipolar transistor process using sidewall spacer for aligning base insert
Colinge, Jean-Pierre / Hewlett-Packard Company, *EUROPEAN PATENT*, Aug 1989
...steps of: forming a **polysilicon emitter** contact pedestal on...chemically removed. A heavy **arsenic**, or other n-type dopant such as **antimony**, implant penetrates...5A, including the **polysilicon emitter** contact pedestal 204...
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☐ **37.** A VLSI self-aligned bipolar transistor
Brighton, Jeffrey E. / TEXAS INSTRUMENTS INCORPORATED, *EUROPEAN PATENT*, Jan 1988
...base region is self-aligned to a **polysilicon emitter** and which defines the emitter region...thermally oxidizing the edge of the N+ **polysilicon emitter** which makes junction depth control...transistor structure in which a doped **polysilicon emitter** contact, used to form a self-aligned...
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☐ **38.** Semiconductor transistor
Morishita, Masakazu / Sugawa, Shigetoshi / Koizumi, Toru / CANON KABUSHIKI KAISHA, *EUROPEAN PATENT*, Mar 1994
...emitter and the case of forming a bipolar transistor of a **polysilicon emitter** are shown, respectively. As will be understood from Fig...process. In case of forming a bipolar transistor of a **polysilicon emitter**, six masks are added to the standard CMOS process. Consequently...
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☐ **39.** Integrated bipolar and CMOS transistor fabrication process
Shah, Rajiv R. / Tran, Toan / TEXAS INSTRUMENTS INCORPORATED, *EUROPEAN PATENT*, Aug 1988
...defining CMOS transistor gate conductors and the bipolar **polysilicon emitter** region. The heavily doped thick polysilicon forms the...bipolar transistor. In forming the walled emitter, the **polysilicon emitter** is in contact with the transition region between the field...
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☐ **40.** Method for producing a buried contact Schottky logic array, and device produced thereby
Morris, Francis J. / Evans, Stephen A. / TEXAS INSTRUMENTS INCORPORATED, *EUROPEAN PATENT*, Jun 1987
...patterned and heavily implanted with **arsenic** to make them N-type. Layer 45 is then...The poly layer 45 may be implanted with **arsenic** and annealed before it is patterned. The anneal diffuses the **arsenic** out of the polysilicon bodies 46 and...
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☐ **41.** Method for producing a poly emitter logic array, and device produced thereby
Morris, Francis J. / Evans, Stephen A. / TEXAS INSTRUMENTS INCORPORATED, *EUROPEAN PATENT*, Apr 1987
...areas, and an N-type dopant such as **antimony** is implanted into collector 12 and resistor...atmosphere. This anneal step activates the **antimony** to turn areas 12 and 14 into N+ doped regions. During the **antimony** anneal, heavily doped regions 12 and...
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☐ **42.** Semiconductor integreated circuit device and method of manufacturing the same
Iwasaki, Hiroshi / KABUSHIKI KAISHA TOSHIBA, *EUROPEAN PATENT*, Sep 1986
...semiconductor device described above, **arsenic** is doped in a polysilicon...by diffusion from the doped **polysilicon emitter** electrode. EP-A-0 03 43 41...an N-type impurity such as **antimony** (Sb) is diffused into the...process shown in Fig. 1E, **arsenic** is doped in regions 29, 30...
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☐ **43.** An improved twin-well BiCMOS process
Eklund, Robert H. / Havemann, Robert H. / Haken, Roger A. / Scott, David B. / TEXAS INSTRUMENTS INCORPORATED, *EUROPEAN PATENT*, Jun 1989
...diffusion of dopant from the **polysilicon emitter** contact which makes contact...by making contact to the **polysilicon emitter** electrode at a location...is typically required for **antimony** diffusion. The resultant...course other dopants such as **arsenic** may be used to form buried...
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☐ **44.** A bicmos process for forming self-aligned NPN emitters and bases and mosfet/source drains
Havemann, Robert H. / TEXAS INSTRUMENTS INCORPORATED, *EUROPEAN PATENT*, Dec 1988
...defined in the substrat and then a doped **polysilicon emitter** and poly gates are

formed in the bipolar...formed by implanting an impurity such as **antimony** into the substrate with a dose of about...implanted with n-type impurity such as **arsenic** at a dosage of approximately 1.0 x 10...

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